Amend claim 29 as follows:

29. (Amended) The method of claim 28, further comprising the steps of:

forming sidewall spacers on opposite sides of the polysilicon gate structures;

further implanting the source/drain regions associated with the low and high voltage NMOS devices using a phosphorus or arsenic implantation [process]; and

further implanting the source/drain regions associated with the low and high voltage PMOS devices using a boron implantation [process].

Amend claim 30 as follows:

30. (Amended) The method of claim 29, further comprising the steps of:

forming a first gate oxide layer having a first thickness overlying the active regions associated with the low voltage NMOS and PMOS devices; and

forming a second gate oxide layer having a second thickness overlying the active regions associated with high voltage NMOS and PMOS devices, wherein the second thickness is greater than the first thickness.

REMARKS

Claims 1 to 4, 6, 7, 10, 12, 13, 16, 17 to 22 and 25 to 30 have been amended. Claims 1 to 30 remain active in this application.

Claims 1 to 30 were rejected under 35 U.S.C. 112, second paragraph, as being indefinite. These claims have been amended to overcome this rejection.

Claims 1 to 17 were rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. (U.S. 6,297,082) in view of Takahashi (U.S. 6,188,109). The rejection is respectfully traversed.

Claim 1 requires, among other features, implanting a first transistor region associated with a first transistor device in the semiconductor device substrate to adjust a threshold voltage associated with the first transistor device and concurrently implanting a portion of a second transistor region in the semiconductor device substrate associated with a second transistor device in the semiconductor device to form source/drain regions associated with the second transistor device with a channel region between the source/drain regions. No such step is taught or suggested by Lin et al., Takahashi or any proper combination of these references either alone or in the combination as claimed.

Claim 1 further requires the step of then forming a first gate oxide structure overlying a channel region in the first transistor region, the first gate oxide structure having a first thickness and forming a second gate oxide structure overlying the channel region in the second transistor region, the second gate oxide structure having a second thickness, the second thickness being greater than the first thickness. No such step is taught or suggested by Lin et al., Takahashi or any proper combination of these references either alone or in the combination as claimed.

Claims 2 to 17 depend from claim 1 and therefore define patentably over the applied references for at least the reasons presented above with reference to claim 1.

a portion of the first transistor region to form source/drain regions associated with the first transistor device. No such step is taught or suggested by Lin et al., Takahashi or any proper combination of these references either alone or in the combination as claimed.

Claim 3 further limits claim 2 by requiring the steps of then implanting a third transistor region associated with a third transistor device in the semiconductor device

substrate to adjust a threshold voltage associated with the third transistor device and concurrently implanting a portion of a fourth transistor region in the semiconductor device substrate associated with a fourth transistor device in the semiconductor device to form source/drain regions associated with the fourth transistor device with a channel region between said source/drain regions [using the third implantation process] and then forming a third gate oxide structure overlying a channel region in the third transistor region, the third gate oxide structure having a third thickness and forming a fourth gate oxide structure overlying the channel region in the fourth transistor region, the fourth gate oxide structure having a fourth thickness, the fourth thickness being greater than the third thickness. No such steps are taught or suggested by Lin et al., Takahashi or any proper combination of these references either alone or in the combination as claimed.

Claim 4 further limits claim 3 by requiring the step of implanting a portion of the third transistor region to form a source/drain region associated with the third transistor device. No such step is taught or suggested by Lin et al., Takahashi or any proper combination of these references in the combination as claimed.

Claim 5 further limits claim 3 by requiring that the first and third transistor devices comprise a first one of an NMOS transistor and a PMOS transistor and the

PMOS transistor. No such step is taught or suggested by Lin et al., Takahashi or any proper combination of these references in the combination as claimed.

Claim 6 further limits claim 3 by requiring that the first and third transistor devices comprise NMOS transistors and the second and fourth transistor devices comprise PMOS transistors, and wherein implanting the third transistor region and a

portion of the fourth transistor region comprises implanting phosphorus in the third transistor region and a portion of the fourth transistor region. No such step is taught or suggested by Lin et al., Takahashi or any proper combination of these references in the combination as claimed.

Claim 7 further limits claim 6 by requiring that implanting phosphorus in the third transistor region and a portion of the fourth transistor region comprise the steps of performing a phosphorus threshold adjustment implantation in the third transistor region and a portion of the fourth transistor region using a dose of about 8 E11 cm^{-2} and an energy of about 20 keV and performing a phosphorus punch-through implantation in the third transistor region and a portion of the fourth transistor region using a dose of about 2 E12 cm^{-2} and an energy of about 70 keV. No such step is taught or suggested by Lin et al., Takahashi or any proper combination of these references in the combination as claimed.

Claim 8 further limits claim 4 by requiring that the first and third transistor devices comprise NMOS transistors and the second and fourth transistor devices comprise PMOS transistors, and wherein implanting a portion of the third transistor region using the fourth implantation process comprises implanting boron in a portion of

or any proper combination of these references in the combination as claimed.

Claim 9 further limits claim 8 by requiring that implanting boron in a portion of the fourth transistor region comprise performing a boron LDD implantation in a portion of the fourth transistor region using a dose of about 4 E13 cm^{-2} and an energy of about 20

keV. No such step is taught or suggested by Lin et al., Takahashi or any proper combination of these references in the combination as claimed.

Claim 10 further limits claim 2 by requiring that the first transistor device comprise an NMOS transistor and the second transistor device comprises a PMOS transistor, and wherein implanting a portion of the first transistor region comprises implanting at least one of phosphorus and arsenic in a portion of the first transistor region. No such step is taught or suggested by Lin et al., Takahashi or any proper combination of these references in the combination as claimed.

Claim 11 further limits claim 10 by requiring that implanting at least one of phosphorus and arsenic in a portion of the first transistor region comprise performing a phosphorus LDD implantation in a portion of the first transistor region using a dose of about 4 E13 cm^{-2} and an energy of about 40 keV. No such step is taught or suggested by Lin et al., Takahashi or any proper combination of these references in the combination as claimed.

Claim 12 further limits claim 1 by requiring that the first transistor device comprise an NMOS transistor and the second transistor device comprise a PMOS transistor, and wherein implanting the first transistor region and a portion of the second

the second transistor region. No such step is taught or suggested by Lin et al., Takahashi or any proper combination of these references in the combination as claimed.

Claim 13 further limits claim 12 by requiring that implanting boron in the first transistor region and a portion of the second transistor region comprise the steps of performing a boron threshold adjustment implantation in the first transistor region and a

portion of the second transistor region using a dose of about 3 E12 cm^{-2} and an energy of about 20 keV and performing a boron punch-through implantation in the first transistor region and a portion of the second transistor region using a dose of about 4 E12 cm^{-2} and an energy of about 70 keV. No such step is taught or suggested by Lin et al., Takahashi or any proper combination of these references in the combination as claimed.

Claim 14 further limits claim 1 by requiring that the first thickness be about 65 Å or more and the second thickness be about 300 Å or less. No such step is taught or suggested by Lin et al., Takahashi or any proper combination of these references in the combination as claimed.

Claim 15 further limits claim 14 by requiring that the first thickness be about 75 Å and the second thickness be about 200 Å. No such step is taught or suggested by Lin et al., Takahashi or any proper combination of these references in the combination as claimed.

Claim 16 further limits claim 1 by requiring that the first transistor device comprise a PMOS transistor and the second transistor device comprise an NMOS transistor, and wherein implanting the first transistor region and a portion of the second transistor region using the first implantation process comprises implanting phosphorus in

taught or suggested by Lin et al., Takahashi or any proper combination of these references in the combination as claimed

Claim 17 further limits claim 16 by requiring that implanting phosphorus in the first transistor region and a portion of the second transistor region comprise the steps of performing a phosphorus threshold adjustment implantation in the first transistor region

and a portion of the second transistor region using a dose of about 8 E11 cm^{-2} and an energy of about 20 keV and performing a phosphorus punch-through implantation in the first transistor region and a portion of the second transistor region using a dose of about 2 E12 cm^{-2} and an energy of about 70 keV. No such step is taught or suggested by Lin et al., Takahashi or any proper combination of these references in the combination as claimed.

Claims 18 to 25 were rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Takahashi. The rejection is respectfully traversed.

Claim 18 requires, the step of adjusting a threshold voltage of a first transistor device in a first region of said semiconductor device substrate and concurrently forming a source/drain region of a second transistor device, both using the same implant. No such step is taught or suggested by Lin et al., Takahashi or any proper combination of these references either alone or in the combination as claimed.

Claims 19 to 25 depend from claim 18 and therefore define patentably over the applied references for at least the reasons presented above with reference to claim 181

In addition, claim 19 further limits claim 18 by requiring the step of forming a source/drain region of the first transistor device. No such step is taught or suggested by

claimed.

Claim 20 further limits claim 19 by requiring the steps of then forming a first gate oxide structure of the first transistor device having a first thickness and forming a second gate oxide structure of the second transistor device having a second thickness, the second thickness being greater than the first thickness. No such step is taught or suggested by

Lin et al., Takahashi or any proper combination of these references either alone or in the combination as claimed.

Claim 21 further limits claim 19 by requiring the steps of then adjusting a threshold voltage of a third transistor device and forming a source/drain region of a fourth transistor device. No such step is taught or suggested by Lin et al., Takahashi or any proper combination of these references either alone or in the combination as claimed.

Claim 22 further limits claim 21 by requiring the steps of forming a source/drain region of the third transistor device using a second LDD implantation process. No such step is taught or suggested by Lin et al., Takahashi or any proper combination of these references in the combination as claimed.

Claim 23 further limits claim 22 by requiring that the first and third transistor devices comprise a first one of NMOS transistors and PMOS transistors and the second and fourth transistors comprise a second one of NMOS transistors and PMOS transistors. No such step is taught or suggested by Lin et al., Takahashi or any proper combination of these references in the combination as claimed.

Claim 24 further limits claim 18 by requiring that the first transistor device comprise an NMOS transistor and the second transistor device comprise a PMOS

forming a source/drain region of the second transistor device using the first threshold adjust implantation process comprises selectively implanting a first transistor region associated with the first transistor device to adjust a threshold voltage associated with the first transistor device, and implanting a portion of a second transistor region associated with the second transistor device to form a source/drain region associated with the second

transistor device using boron. No such step is taught or suggested by Lin et al., Takahashi or any proper combination of these references in the combination as claimed.

Claim 25 further limits claim 18 by requiring that the first transistor device comprise a PMOS transistor and the second transistor device comprise an NMOS transistor, and wherein adjusting a threshold voltage of the first transistor device and forming a source/drain region of the second transistor device comprises selectively implanting a first transistor region associated with the first transistor device to adjust a threshold voltage associated with the first transistor device, and implanting a portion of a second transistor region associated with the second transistor device to form a source/drain region associated with the second transistor device using phosphorus.

Claims 26 and 27 were rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Takahashi. The rejection is respectfully traversed.

Claim 26 requires, among other features, selectively concurrently implanting a first transistor region in the semiconductor device substrate to adjust a threshold voltage associated with a first transistor device and a portion of a second transistor region to form a source/drain region associated with a second transistor device. No such step is taught or suggested by Lin et al., Takahashi or any proper combination of these references either

Claim 27 depends from claim 26 and therefore defines patentably over the applied references for at least the reasons set forth above with reference to claim 26.

Claim 27 further limits claim 26 by requiring that the step of selectively implanting the first transistor region and a portion of the second transistor region comprise the step of implanting one of phosphorus, arsenic and boron in the first

transistor region and a portion of the second transistor region. No such step is taught or suggested by Lin et al., Takahashi or any proper combination of these references in the combination as claimed.

Claims 28 to 30 were rejected under 35 U.S.C.103(a) as being unpatentable over Lin et al. in view of Takahashi. The rejection is respectfully traversed.

Claim 28 requires, among other features, the steps of concurrently implanting an active region of a low voltage NMOS device and source/drain regions of a high voltage PMOS device using a boron threshold voltage adjust implantation, then concurrently implanting an active region of a low voltage PMOS device and source/drain regions of a high voltage NMOS device using a phosphorus threshold voltage adjust implantation, then forming polysilicon gate structures associated with the high and low voltage NMOS and PMOS devices, then implanting source/drain regions associated with the low voltage NMOS device using a phosphorus or arsenic LDD implantation and then implanting source/drain regions associated with the low voltage PMOS device using a boron LDD implantation. No such steps are taught or suggested by Lin et al., Takahashi or any proper combination of these references either alone or in the combination as claimed.

Claims 29 and 30 depend from claim 28 and therefore define patentably over the

Claim 29 further limits claim 28 by requiring the steps of forming sidewall spacers on opposite sides of the polysilicon gate structures, further implanting the source/drain regions associated with the low and high voltage NMOS devices using a phosphorus or arsenic implantation and further implanting the source/drain regions associated with the low and high voltage PMOS devices using a boron implantation. No

such step is taught or suggested by Lin et al., Takahashi or any proper combination of these references in the combination as claimed.

Claim 30 further limits claim 29 by requiring the steps of forming a first gate oxide layer having a first thickness overlying the active regions associated with the low voltage NMOS and PMOS devices and forming a second gate oxide layer having a second thickness overlying the active regions associated with high voltage NMOS and PMOS devices, wherein the second thickness is greater than the first thickness. No such step is taught or suggested by Lin et al., Takahashi or any proper combination of these references in the combination as claimed.

In view of the above remarks, favorable reconsideration and allowance are respectfully requested.

Respectfully submitted,

Jay M. Cantor
Reg. No. 19906
(202) 639-7713

1. A method of fabricating MOSFET transistors in a semiconductor device, comprising the steps of:

providing a semiconductor device substrate;

implanting a first transistor region associated with a first transistor device in the semiconductor device substrate to adjust a threshold voltage associated with the first transistor device and concurrently implanting a portion of a second transistor region in the semiconductor device substrate associated with a second transistor device in the semiconductor device to form source/drain regions associated with the second transistor device with a channel region between said source/drain regions;

then forming a first gate oxide structure overlying a channel region in the first transistor region, the first gate oxide structure having a first thickness and forming a second gate oxide structure overlying the channel region in the second transistor region, the second gate oxide structure having a second thickness, the second thickness being greater than the first thickness.

2. The method of claim 1, further comprising the step of then implanting a portion of the first transistor region to form source/drain regions associated with the first transistor device.

3. The method of claim 2, further comprising the steps of then implanting a third transistor region associated with a third transistor device in the semiconductor device substrate to adjust a threshold voltage associated with the third transistor device and concurrently implanting a portion of a fourth transistor region in the semiconductor device substrate associated with a fourth transistor device in the semiconductor device to form source/drain regions associated with the fourth transistor device with a channel region between said source/drain regions;

then forming a third gate oxide structure overlying a channel region in the third transistor region, the third gate oxide structure having a third thickness and forming a fourth gate oxide structure overlying the channel region in the fourth transistor region, the fourth gate oxide structure having a fourth thickness, the fourth thickness being greater than the third thickness.

4. The method of claim 3, further comprising the step of implanting a portion of the third transistor region to form a source/drain region associated with the third transistor device.

5. The method of claim 3, wherein the first and third transistor devices comprise a

fourth transistor devices comprise a second one of an NMOS transistor and a PMOS transistor.

6. The method of claim 3, wherein the first and third transistor devices comprise NMOS transistors, wherein the second and fourth transistor devices comprise PMOS transistors, and wherein implanting the third transistor region and a portion of the fourth transistor region comprises implanting phosphorus in the third transistor region and a portion of the fourth transistor region.

7. The method of claim 6, wherein implanting phosphorus in the third transistor region and a portion of the fourth transistor region comprises the steps of:

performing a phosphorus threshold adjustment implantation in the third transistor region and a portion of the fourth transistor region using a dose of about 8 E11 cm^{-2} and an energy of about 20 keV; and

performing a phosphorus punch-through implantation in the third transistor region and a portion of the fourth transistor region using a dose of about 2 E12 cm^{-2} and an energy of about 70 keV.

8. The method of claim 4, wherein the first and third transistor devices comprise NMOS transistors, wherein the second and fourth transistor devices comprise PMOS transistors, and wherein implanting a portion of the third transistor region using the fourth

region.

9. The method of claim 8, wherein implanting boron in a portion of the fourth transistor region comprises performing a boron LDD implantation in a portion of the fourth transistor region using a dose of about 4 E13 cm^{-2} and an energy of about 20 keV.

10. The method of claim 2, wherein the first transistor device comprises an NMOS transistor, wherein the second transistor device comprises a PMOS transistor, and wherein implanting a portion of the first transistor region comprises implanting at least one of phosphorus and arsenic in a portion of the first transistor region.

11. The method of claim 10, wherein implanting at least one of phosphorus and arsenic in a portion of the first transistor region comprises performing a phosphorus LDD implantation in a portion of the first transistor region using a dose of about 4 E13 cm^{-2} and an energy of about 40 keV.

12. The method of claim 1, wherein the first transistor device comprises an NMOS transistor, wherein the second transistor device comprises a PMOS transistor, and wherein implanting the first transistor region and a portion of the second transistor region comprises implanting boron in the first transistor region and a portion of the second transistor region.

13. The method of claim 12, wherein implanting boron in the first transistor region and a portion of the second transistor region comprises the steps of:

performing a boron threshold adjustment implantation in the first transistor region and a portion of the second transistor region using a dose of about 5 E12 cm^{-2} and an energy of about 20 keV; and

performing a boron punch-through implantation in the first transistor region and a portion of the second transistor region using a dose of about 4 E12 cm^{-2} and an energy of about 70 keV.

14. The method of claim 1, wherein the first thickness is about 65 Å or more and the second thickness is about 300 Å or less.

15. The method of claim 14, wherein the first thickness is about 75 Å and the second thickness is about 200 Å.

16. The method of claim 1, wherein the first transistor device comprises a PMOS transistor, wherein the second transistor device comprises an NMOS transistor, and wherein implanting the first transistor region and a portion of the second transistor region using the first implantation process comprises implanting phosphorus in the first transistor region and a portion of the second transistor region.

17. The method of claim 16, wherein implanting phosphorus in the first transistor region and a portion of the second transistor region comprises the steps of:

performing a phosphorus threshold adjustment implantation in the first transistor region and a portion of the second transistor region using a dose of about 8 E11 cm^{-2} and an energy of about 20 keV; and

performing a phosphorus punch-through implantation in the first transistor region and a portion of the second transistor region using a dose of about 2 E12 cm^{-2} and an energy of about 70 keV.

18. A method of fabricating MOSFET transistors in a semiconductor device, comprising the steps of:

providing a semiconductor device substrate;

adjusting a threshold voltage of a first transistor device in a first region of said semiconductor device substrate; and concurrently forming a source/drain region of a second transistor device, both using the same implant.

19. The method of claim 18, further comprising the step of forming a source/drain region of the first transistor device.

20. The method of claim 19, further comprising the steps of:

then forming a first gate oxide structure of the first transistor device having a first thickness, and

forming a second gate oxide structure of the second transistor device having a second thickness, the second thickness being greater than the first thickness.

21. The method of claim 19, further comprising the steps of then adjusting a threshold voltage of a third transistor device and forming a source/drain region of a fourth transistor.

22. The method of claim 21, further comprising the steps of forming a source/drain region of the third transistor device using a second LDD implantation process.

23. The method of claim 22, wherein the first and third transistor devices comprise a first one of NMOS transistors and PMOS transistors, and wherein the second and fourth transistors comprise a second one of NMOS transistors and PMOS transistors.

24. The method of claim 18, wherein the first transistor device comprises an NMOS transistor, wherein the second transistor device comprises a PMOS transistor, and wherein adjusting a threshold voltage of the first transistor device and forming a source/drain region of the second transistor device using the first threshold adjust implantation process comprises selectively implanting a first transistor region associated with the first transistor device to adjust a threshold voltage associated with the first transistor device, and implanting a portion of a second transistor region associated with the second transistor device to form a source/drain region associated with the second transistor device using boron.

25. The method of claim 18, wherein the first transistor device comprises a PMOS transistor, wherein the second transistor device comprises an NMOS transistor, and wherein adjusting a threshold voltage of the first transistor device and forming a source/drain region of the second transistor device comprises selectively implanting a

voltage associated with the first transistor device, and implanting a portion of a second transistor region associated with the second transistor device to form a source/drain region associated with the second transistor device using phosphorus.

26. A method of forming a source/drain region in a semiconductor device, comprising the steps of:

providing a semiconductor device substrate; and

selectively concurrently implanting a first transistor region in said semiconductor device substrate to adjust a threshold voltage associated with a first transistor device and a portion of a second transistor region to form a source/drain region associated with a second transistor device.

27. The method of claim 26, wherein selectively implanting the first transistor region and a portion of the second transistor region comprises the step of implanting one of phosphorus, arsenic and boron in the first transistor region and a portion of the second transistor region.

28. A method of fabricating a semiconductor device, comprising the steps of:

providing a semiconductor device substrate;

concurrently implanting in said semiconductor device substrate an active region of a low voltage NMOS device and source/drain regions of a high voltage PMOS device using a boron threshold voltage adjust implantation;

then concurrently implanting in said semiconductor device substrate an active region of a low voltage PMOS device and source/drain regions of a high voltage NMOS device using a phosphorus threshold voltage adjust implantation;

forming polysilicon gate structures associated with the high and low voltage NMOS and PMOS devices,

implanting source/drain regions associated with the low voltage NMOS device using a phosphorus or arsenic LDD implantation; and

implanting source/drain regions associated with the low voltage PMOS device using a boron LDD implantation.

29. The method of claim 28, further comprising the steps of:

forming sidewall spacers on opposite sides of the polysilicon gate structures;

further implanting the source/drain regions associated with the low and high

[illegible] implantation [process]; and

further implanting the source/drain regions associated with the low and high voltage PMOS devices using a boron implantation.

30. The method of claim 29, further comprising the steps of:

forming a first gate oxide layer having a first thickness overlying the active regions associated with the low voltage NMOS and PMOS devices; and

forming a second gate oxide layer having a second thickness overlying the active regions associated with high voltage NMOS and PMOS devices, wherein the second thickness is greater than the first thickness.